# A two-stage time-to-digital converter based on cyclic pulse shrinking

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*Abstract*— **The design of a novel time-to-digital converter based on the cyclic pulse shrinking method and implemented in an FPGA (*Field Programmable Gate Array*) device is proposed. The pulse shrinking is realized by two complementary delay lines made as built-in carry chains. In the first line the noninverted pulse is being shrunk while in the second one the inverted pulse is being stretched. The converter resolution depends on the length ratio of the lines. To avoid the influence of any circuit element apart from the lines on the resolution, the information about a measured time interval is transmitted between the lines as a time interval between two pulses representing the leading and trailing edges of the original pulse. To increase the precision of converter a two-stage conversion is introduced. The low-resolution first stage shortens substantially the conversion time and provides a wide measurement range whereas the second stage provides a high resolution. The designed two-stage converter has a resolution of 42 ps and the measurement uncertainty below 56 ps within the whole measurement range. The two-stage structure is obtained as modification of a single-stage converter featuring the resolution of 75 ps and the maximum measurement uncertainty of 150 ps, which is also described in this paper.**

## I. INTRODUCTION

Direct time coding with the use of a tapped delay line is the most popular method of time digitizing [1]. The conversion is fast and its practical realization is relatively easy, however reaching the high resolution strongly depends on the technology used. The highest resolution at a level of a few tens of picoseconds [2, 3] is achievable in digitizers implemented in CMOS ASIC (*Application Specific Integrated Circuit*) devices while FPGA-based converters provide resolution at a level of several tens of picoseconds [4, 5]. The method giving possibility to achieve potentially unlimited high resolution is the pulse shrinking [1, 6]. Simplified block diagram of a converter based on the pulse shrinking principle is shown in fig. 1.

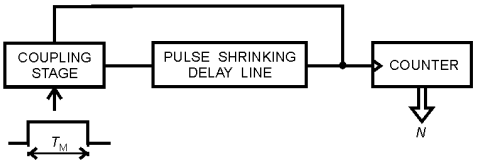


Figure 1. Conceptual block diagram of the time-to-digital converter based on cyclic pulse shrinking.

The measured time interval $T_M$ is represented in this method as the width time of a pulse. The pulse is launched into a delay loop through a coupling stage. The coupling stage should be such designed to introduce equal delays for both pulse edges ($t_{PLH} = t_{PHL}$), whereas the pulse shrinking delay line (PShDL) has to delay the rising pulse edge longer than the falling one ($t_{PLH} > t_{PHL}$). In this way the width time of the pulse circulating in the loop is reduced after each cycle by a constant amount of time equaled to the difference $t_{PLH} - t_{PHL}$. The counter counts subsequent cycles in the loop until the pulse disappears. The value of measured time interval is calculated as $T_M = NR$, where $N$ is the total number of cycles and $R = (t_{PLH} - t_{PHL})$ is the resolution of converter.

To date the pulse shrinking method was utilized in converters implemented in custom-designed CMOS IC's [7 – 10] due to merits of this technology such as possibility for independent and precise control of internal propagation times for both pulse edges what, in turn, allows for controlling the converter resolution. However, the development cycle time of custom designed IC's is long and their costs are relatively large. In addition any design modifications are not easy to introduce. Taking these drawbacks into consideration the *Field Programmable Gate Array* (FPGA) devices appears as a desirable alternative. Since in the FPGA devices a designer can not control the delay time of logic gate by e.g. bias adjustments, an implementation of such a method of conversion is much more complicated. However, modern FPGAs are packed with features that were not previously available such as fast carry chains having short and similar delay times for both pulse edges. They create possibility to

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design a pulse-shrinking-based converter with a high resolution and wide measurement range.

## II. CONVERTER DESIGN

### A. Converter Based on Single-Stage Pulse Shrinking

As a first approach we designed a time-to-digital converter based on a single-stage conversion principle. Its simplified block diagram is shown in fig. 2a.

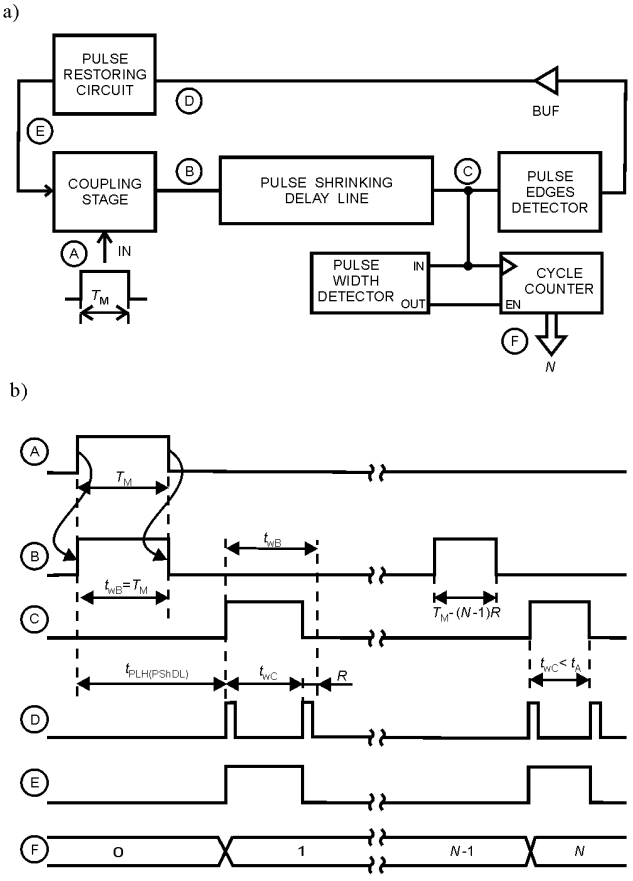


Figure 2. Block diagram of the single-stage converter (a) and related waveforms (b).

The converter is implemented in an FPGA device from the series Spartan-3 (*Xilinx*). Carry chains in the Spartan-3 devices contain multiplexers which provide similar propagation times for both pulse edges. Therefore they can be used to construct a relatively long delay line which does not shrink or stretch propagating pulse excessively. Otherwise the pulse would disappear before it reaches the end of the line. Since built-in carry chain contains 128 multiplexers having average delay time of about 45 ps thus each carry chain is a line with the delay of about 5.8 ns. Such a carry chain was used as the PShDL in our design. In order to minimize the influence of any element of loop other than PShDL on the width of pulse, beyond the PShDL both edges of the pulse are represented by the rising edges of two short pulses. In this way circuit elements, apart from the PShDL, introduce equal delays for both pulses and do not change value of the measured time interval. The change of representation of the measured time interval from the pulse width to the time interval between two pulses is provided by the pulse edges detector (fig. 2a). The pulses obtained from the output of detector are transmitted to the input of pulse restoring circuit through the global buffer and fast global path. Such solution minimizes a number of connecting switch matrices and path segmentation. The pulse restoring circuit provides reverse operation to the pulse edges detector and restores the pulse to its original shape. Then the pulse is again applied to the input of PShDL through the coupling stage. As the simplest coupling stage a two-input OR gate may be used.

The pulse circulating within the loop is being gradually shrunk until it reaches the minimum width time $t_A$ detected in the pulse width detector (fig. 2a). The number of cycles $N$ in the loop is counted by the cycle counter. The measured time interval is calculated as $T_M = N\ R + t_A$. The pulse width threshold $t_A$ is treated as an offset and should be estimated during a calibration of the converter. Waveforms illustrating the conversion process are presented in fig. 2b.

During the first test of the designed converter we determined its transfer characteristic and verified accuracy. In order to do this we checked numbers of cycles in the loop counted for different input time intervals within the range up to 6 ns. The intervals were obtained with the use of a set of precisely cut coaxial cables, with delays differing by about 300 ps. Mean values of numbers of cycles, each obtained from sample size of 1000, were used to determine the transfer characteristic of the converter (triangles in fig. 3). The average resolution of the converter equals 75 ps and was calculated as a quotient of the measurement range (5.5 ns) and the total increase in the number of cycles (73.5) corresponding to maximal change of the measured time interval. The measurement uncertainty of the converter (squares in fig. 3) gradually increases with the measured time interval from about 40 ps up to 150 ps. This effect is caused by the jitter of edges of the pulse circulating in loop. The value of the jitter increases roughly as the square root of the time of observation [11, 12], i.e. the measured time interval.

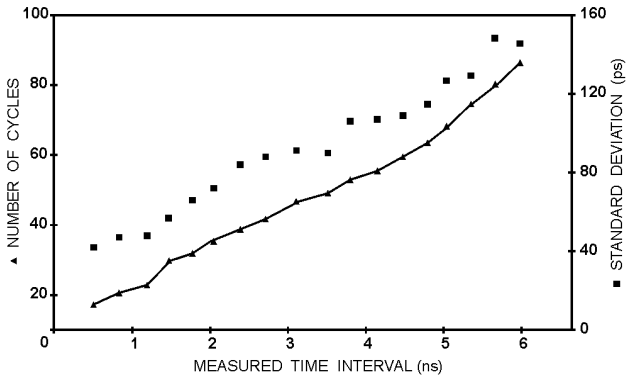


Figure 3. Transfer characteristic (triangles) and standard measurement uncertainty (squares) of the single-stage converter.

The single-stage converter described above is relatively easy for implementation in integrated circuits. However, it suffers from a serious disadvantage. Its measurement uncertainty increases along with the measured time interval. To raise the resolution and lower the measurement

uncertainty of the converter we propose a novel two-stage its structure.

### B. *Converter Based on Two-Stage Pulse Shrinking*

The second converter consists of two conversion stages built as delay loops of different lengths. The first conversion stage (FCS) is based on the longer delay loop (loop A – blue color in fig. 4) that contains two delay lines (shrinking and stretching), two pulse edges detectors (A and B) and two pulse restoring circuits (A). The measured pulse is launched into the loop as noninverted and is shrunk in the PShDL. Then the pulse is inverted and is stretched in the pulse stretching delay line (PStDL). Both lines consist of the same number of delay elements and thus any changes in the pulse width are virtually eliminated. For the same reason mentioned in the case of the single stage converter, at outputs of both delay lines the circulating pulse is converted into two short pulses by the pulse edges detectors. Additionally the pulse edges detector A delays the leading pulse longer than the trailing one, and thus shortens substantially the time interval between them. The scale of shortening decides about the course resolution $R$ of the converter. To diminish the jitter of pulse edges, and to improve the measurement uncertainty of converter, the duration of conversion should be possibly short [11]. Therefore the value of FCS resolution should be relatively large (e.g. 1 ns) resulting in significant shrinking of the circulating pulse after each cycle and consequently in limitation of a number of cycles. The number is counted by the counter A.

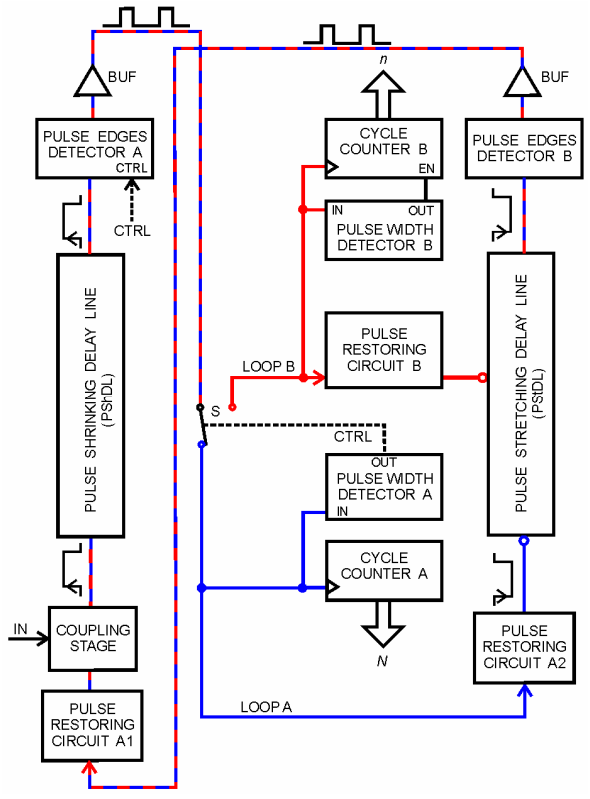


Figure 4. Simplified block diagram of the two-stage converter.

When the pulse width becomes shorter then the minimum width $t_A$ detected by the pulse width detector A, the configuration of the converter is changed. The switch S opens the longer loop A and closes the shorter loop B (red color in fig. 4). The latter loop is the second conversion stage (SCS) which operates similarly as the FCS and contains mostly the same elements. Due to change in the converter configuration, the pulse restoring circuit A2 is substituted by the pulse restoring circuit B and only part of the PStDL is now utilized. Shortened PStDL only partially compensates the pulse shrinking caused by the PShDL and the uncompensated value of shrinking is the fine resolution $r$ of converter. The pulse edges detector A, while operates in the SCS, does not influence the pulse width (being disabled by the signal CTRL). The value of fine resolution is proportional to the difference in length of both lines and can be controlled by the change of location of the pulse restoring circuit B relative to the original input of the PStDL. If the circuit is located closer to the input the "active" length of the PStDL is longer and consequently the value of resolution is smaller. The pulse circulating in the loop B is now shortened by $r << R$ after each cycle. The circulation is stopped when the pulse width becomes shorter than the minimum width $t_B$ detected by the pulse width detector B. Number of cycles $n$ in the loop B is counted by the cycle counter B. The value of measured time interval is calculated as $T_M = N\,R + n\,r + t_B$, where the pulse width threshold $t_B$ is evaluated in the same manner as $t_A$ for the single-stage converter.

## III. Test Results

The designed converter was implemented in the Spartan-3 device (XC3S400-4PQ208, *Xilinx*). Tests for evaluation of performance of the converter were performed at an ambient room temperature (around 20 °C) and with the use of nominal supply voltages. During the first test we measured a series of time intervals generated by the precise delay generator GFT1004 (*Greenfield Technology*). Each time interval was measured with a sample size of 1000 and calculated mean values were used to plot the transfer characteristic of the converter (triangles in fig. 5). The characteristic is now much more linear than for the single-stage converter. Despite the lack of calibration the experimental results well agree with the theoretical prediction line. The calculated linear correlation coefficient equals 0.9999.

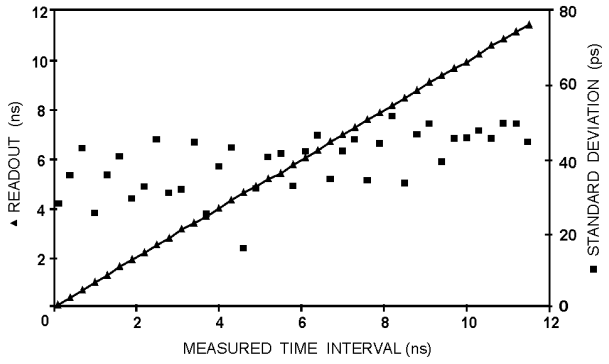


Figure 5. Transfer characteristic (triangles) and standard measurement uncertainty (squares) of the two-stage converter.

To estimate the average value of final resolution *r* of the converter we identified a number of different output codes corresponding to the whole measurement range. The resolution, calculated as a quotient of the range (11.7 ns) and the number of codes (280), equals 42 ps.

Next we evaluted the standard measurement uncertainty of the converter within its measurement range (fig. 5). The maximum value of uncertainty equals 55.8 ps and is almost 3 times smaller than in the case of the single-stage converter. This characteristic of uncertainty also manifests an increase along with the measured time interval but this effect is now much smaller (more than 3 times) and the maximum change in uncertainty does not exceed 35 ps.

The longest conversion time of the two-stage converter equals 710 ns that is about 8 times shorter in comparison with the time of a single-stage converter of the same resolution and measurement range.

## IV. CONCLUSION

Two new time-to-digital converters with single- and two-stage conversion mechanisms are implemented in a reprogrammable FPGA device. The first one has the resolution of 75 ps and the measurement uncertainty below 150 ps. Its simple structure has been greatly improved resulting in two-stage conversion scheme where several techniques are employed to raise both the resolution and accuracy. The crucial meaning has the substantial shortening of the conversion time obtained by the use of coarse and fast pulse shrinking in the first conversion stage. To achieve a high resolution the fine pulse shrinking within a narrow time interval range is provided by two complementary delay lines in the second conversion stage. To avoid an unpredictable shrinking or stretching of a measured pulse by any circuit element apart from the lines (e.g. programmable switches) the information about the pulse width is transmitted between the lines as a time interval between rising edges of two pulses. Eventually, the two-stage converter has a fine resolution of 42 ps and the measurement uncertainty below 56 ps. The use of the two-stage conversion shortened the conversion time almost 8 times in comparison with the single-stage conversion of the same resolution and range. Using mostly the same logical resources of the FPGA device in both conversion stages reduced the area overhead.

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